Photoresist-free printing of amorphous silicon thin-film transistors

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Conventional fabrication of amorphous silicon thin-film transistors (a-Si TFTs) requires patterning numerous photoresist layers, a subtractive process that is time consuming and expensive. This letter describes transistor fabrication by a photoresist-free approach in which polymer etch masks are letterpress printed from flexible polyimide stamps. Pattern registration is achieved through optical alignment since the printed masks are thin and optically transparent. This modified fabrication scheme produces transistor performance equivalent to conventionally fabricated a-Si TFTs. The ability to directly print etch masks onto nonhomogeneous substrates brings one step closer the realization of flexible, large-area, macroelectronic fabrication. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1618364]

The past decade has seen tremendous growth in the number of nonconventional techniques for the fabrication of electronic devices geared toward large-area electronics. These emerging technologies exploit and combine the advantages of conventional printing methods, like those used in high-volume and low cost typographic products, with organic polymer and semiconductor materials for producing flexible and large-scale sensors and displays. The assortment of direct-print techniques includes ink- or wax-jet methods,[1–6] gravure methods,[7] offset-based techniques,[8,9] screen printing,[10,11] surface-chemistry mediated transfer,[12] convective flow assembly,[13] and flexible letterpress stamping (FLEPS).[14]

The FLEPS method has been used to pattern films of polystyrene (PS) and other thermoplastic polymers with micrometer-scale feature sizes. The procedure is highly conducive to pattern transfer on rigid or flexible and flat or curved substrates including glass, silicon, and plastic. Photolithography and etching are used to fabricate the stamp from a 50 μm polyimide foil (DuPont Kapton®E), creating raised features 12 μm high and about 1–100 μm wide; photolithography is not used thereafter.

The schematic diagram in Fig. 1 illustrates the four steps of the printing process. A carrier substrate is spin coated with a PS[15] and toluene solution. In these studies, the PS thickness was chosen to be about 900 nm. The solid film is heated above the glass transition temperature T_g and made to contact a flexible stamp with features defined in relief [Fig. 1(a)]. The stamp is peeled away and cooled to room temperature. The inked stamp is then aligned with a workpiece that may have been prepatterned [Fig. 1(b)]. This assembly is transferred to a hotplate to remelt the PS and facilitate transfer [Figs. 1(c) and 1(d)]. Studies indicate that rapid separation of liquid coated surfaces distributes the coating evenly between the two surfaces.[16] In this study, the final etch mask thickness was estimated to be about 200–250 nm. The polymer films printed in this way are very good masks for both wet and dry etching. The transfer method works well with heterogeneous surfaces and is therefore suited to printing onto workpieces whose surfaces are coated with different materials.

In this letter, we describe how FLEPS has been used to fabricate amorphous silicon thin-film transistors (TFTs) with a bottom-gate structure and the four-layer design shown in Fig. 2. A 100 nm chromium film was deposited by electron-beam (e-beam) evaporation onto a 1.1 mm thick Corning 1737 glass slide. The Cr was patterned as the gate electrode of the TFT by letterpress printing a PS mask and wet etching the unmasked Cr;[17] the PS mask was stripped with toluene and ultrasonic agitation. Films of silicon nitride, intrinsic amorphous silicon (a-Si), and n^+ doped amorphous silicon were then deposited by plasma enhanced chemical vapor deposition (PECVD).[18] E-beam evaporation of a 100 nm Cr film for the top electrodes concluded the deposition sequence.

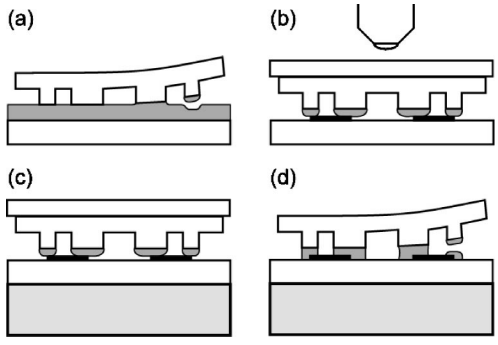

FIG. 1. Schematic diagram of letterpress printing process. (a) Inking of relief features on a polyimide stamp by contact with a molten, spin cast polymer film. (b) Microscope alignment of the inked stamp with a patterned workpiece. The edges of the substrate stack are held in place by glass slides. The two black rectangles represent a previously pattered film. (c) Stack transfer to a hotplate to induce polymer melting and facilitate transfer. (d) Stamp removal leaves printed polymer film.

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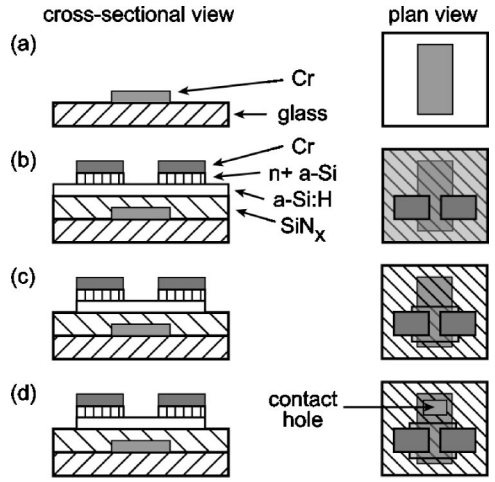

FIG. 2. Cross-sectional and plan views of the a-Si TFT fabrication process. (a) The chromium bottom gate electrode is deposited and patterned by printing and etching. (b) Four additional layers are deposited onto the substrate: Silicon nitride gate dielectric, intrinsic and n^+ doped a-Si layers, and chromium. The chromium and n^+ layers are patterned as the source and drain electrodes. (c) The intrinsic (semiconductor) a-Si island is patterned. (d) A contact hole is opened through the silicon nitride dielectric film for probing the gate electrode.

Alignment of subsequent patterns to the predefined gate electrode was performed manually by gauging registration optically with a microscope. Although the stamp fabrication process roughens the recessed regions of the surface to make them opaque, it leaves the relief portions flat and transparent. When coated with the polymer ink, these regions remain transparent if the polymer surface is smooth. A viscous fingering instability that occurs with feature sizes larger than the instability wavelength ($\sim$12 μm for PS film thickness and mol. wt. used) can, however, generate a rough surface that scatters light. This problem is remedied by heating the polymer above T_g and allowing capillary forces to smooth the film surface. Annealing produced transparent films even for the largest features sizes printed, allowing surfaces with large or small features to be aligned visually.

The source–drain pattern was printed in this way, defining the channel dimensions for the transistor. The Cr film was etched is the same manner as the gate layer. The n^+ a-Si film was then etched by reactive ion etching (RIE)[19] using the same mask, which was then removed. The intrinsic silicon islands and the gate dielectric contact holes were each patterned by printing a PS mask and etching with RIE.

The transistor channel length was designed to be 20 μm. The channel and gate widths were 400 and 170 μm, respectively. An optical micrograph of an a-Si TFT fabricated with letterpress-printed etch masks is shown in Fig. 3. The dimensions for this transistor were chosen to simplify the alignment process; currently, FLEPS can print etch mask films with feature sizes less than 3 μm.[14] Refinement, optimization, and automation of the printing and alignment steps will allow fabrication of etch mask with even smaller feature sizes.

FLEPS fabrication eliminates the need for time-consuming steps like the spin coating of photoresist layers, pre- and postbaking, UV exposure of photoresist through optical masks, and chemical development of photoresist patterns. All of the other processing steps follow a standard photolithography-based fabrication scheme. To compare the performance obtained with the letterpress printed devices, we fabricated two sets of TFTs in parallel—one set by conventional photolithographic processing, the other set using letterpress-printed masks. All deposition and etching steps were carried out simultaneously.

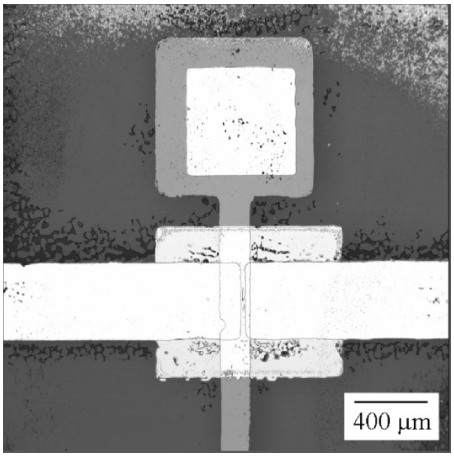

FIG. 3. Optical micrograph of an a-Si TFT fabricated by letterpress printed etch masks. The transistor channel length and width are 20 μm and 400 μm, respectively. The gate width is 170 μm.

Measurements of the electrical performance of TFTs fabricated with the PS etch masks are shown in Fig. 4. The transfer characteristics (the drain current I_d dependence on gate voltage V_g) are shown in Fig. 4(a) for source–drain voltages of V_{ds}=0.1 V and 10 V. Also shown in Fig. 4(a) are the respective gate leakage currents (I_g). The on/off current ratio is about 2×10^6, equivalent to the conventional TFTs. The ratio of the I_d values at V_g=20 V for V_{ds}=0.1 V and

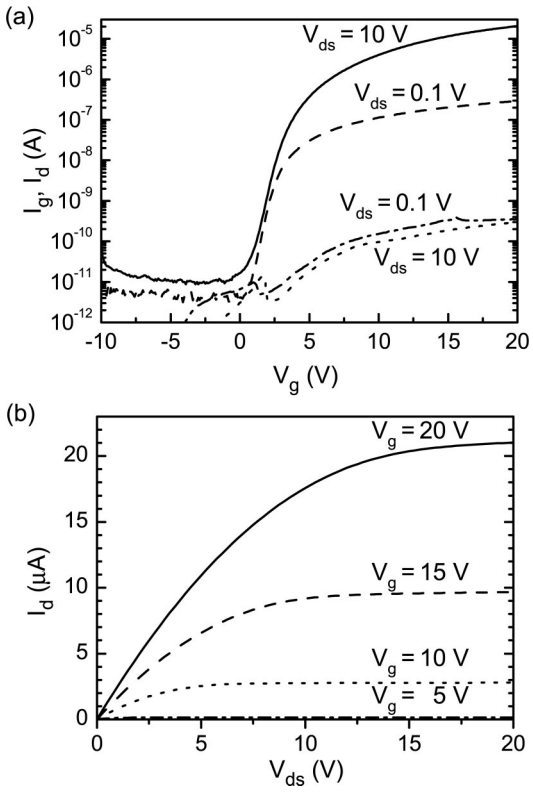

FIG. 4. Device performance of a-Si TFTs fabricated with letterpress-printed etch masks. (a) Transfer characteristics. (b) Output characteristics.

TABLE I. Mean values of electrical characteristics of functioning TFTs fabricated by FLEPS etch masks and by conventional photolithographic processing.

Characteristic	FLEPS	Conventional
$I_{on}/I_{off}(\times 10^6)$	2.1 ±0.9	2.6 ±0.8
μ_{linear} (cm^2/V s)	0.40±0.09	0.26±0.09
μ_{sat} (cm^2/V s)	0.39±0.09	0.28±0.02
$V_{threshold}$ (V)	3.3 ±0.4	3.51±1.7
Subthreshold slope (V/decade)	0.68±0.01	0.80±0.04

10 V is less than 100, suggesting a series resistance. The electron mobilities in the linear (μ_{linear}) and saturation (μ_{sat}) regions, the threshold voltages, and the subthreshold slopes[20,21] for both sets of TFTs are shown in Table I. The output characteristics (I_d as a function of V_{ds}) are plotted in Fig. 4(b); the behavior is linear at low V_{ds}.

We have fabricated functioning *a*-Si TFTs by using directly printed etch masks formed by FLEPS. The electrical performance of these TFTs is equivalent to those fabricated by conventional photolithography. The direct printing of etch masks eliminates several processing steps for each device layer. Because all except the etch mask formation follows standard fabrication procedures, this photoresist-free scheme also allows smooth integration into more traditional process flows. We are currently exploring the use of FLEPS for single-step deposition of functional device layers like gate or interlayer dielectrics. This capability would be especially useful for large-area, electronic, device fabrication.

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[19] RIE of the n^+ doped and intrinsic *a*-Si layers were performed at 150 mTorr using 16 sccm CF_4 at 0.12 W/cm^2. The etch times were determined by observing the interference colors. The silicon nitride films were etched at 100 mTorr using 35 sccm CF_4 and 5 sccm O_2 with 0.16 W/cm^2.
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